Please add the following new claims 16-21 to the application.

16. A gate of electrode/wiring structure as set forth in claim 15, wherein the silicon layer acts as a source for providing silicon with a side wall in the side wall oxidizing step of forming a silicon oxide film on the side wall.

17. A gate of electrode/wiring structure as set forth in claim 15, wherein the tungsten silicide layer comprises a first tungsten silicide layer including a phosphorus atom and a second tungsten silicide layer formed on the first tungsten silicide layer.

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18. A method for preparing a gate electrode/wiring as set forth in claim 8 or 12, wherein the step of depositing a tungsten silicide layer is a step of depositing a tungsten silicide layer including a phosphorus atom on the polysilicon layer.

19. A method for preparing a gate electrode/wiring as set forth in claim 12, wherein the short-time annealing step is an annealing step for preventing silicon atoms from diffusing from the polysilicon layer.

20. A method for preparing a gate electrode/wiring as set forth in claim 12, wherein the step of depositing a tungsten silicide layer on the polysilicon layer comprises a first step of depositing a first tungsten silicide layer including a phosphorus atom on the polysilicon layer and a second step of depositing a second tungsten silicide layer on the first tungsten silicide layer.

21. A method for preparing a gate electrode/wiring as set forth in claim 12, wherein the short time annealing step is carried out for 30 seconds at 1000°C in an atmosphere of 100% nitrogen.